

Sub a

5

and

10

15

block comprises only the pixels in the same column.

20

the pixel block is allocated for the pixel block of N rows \times N' columns.

5. A display method in which a display signal for displaying a picture is independently applied to each of the pixels arranged like the matrix by using the wiring arranged in the directions of column and column, comprising the steps of:

dividing the pixels into pixel blocks of N rows \times N' columns, and

providing signals to the pixels of n lines in a selection period of n times which are less number than N .

6. A display apparatus comprises:

pixel electrodes arranged like a matrix;

display elements which operate according to the voltage of the pixel electrode;

an X driver for supplying an X signal to X signal line arranged in the column direction;

an Y driver for supplying an Y signal to Y signal line arranged in the row direction;

a liquid crystal drive voltage supplying circuit for supplying a liquid crystal drive voltage to a liquid crystal drive voltage line arranged in a column direction;

an XY calculating circuit provided at the intersection

0987619-06001

parts of the X signal line and the Y signal line and connected to the X signal line and the Y signal line for calculating and outputting the X and Y signals;

5 a signal comparator for comparing an output of the XY calculating circuit with a reference voltage and outputting a first voltage when the the output of the XY calculating circuit is higher than the reference voltage, and a second voltage when lower than that;

10 a switch for controlling the connection of the pixel electrode and the liquid crystal drive voltage line, based on the output of the signal comparator;

15 n-gradation approximation calculating circuit for dividing the pixels into pixel blocks of N rows \times N' columns, and converting the gradation level of each pixel of each block into n-gradation approximation picture signal approximated to n values less than $N \times N'$, and

a signal control circuit for controlling the X driver, the Y driver, and liquid crystal drive voltage supplying circuit, according to the n-gradation approximation picture signal.

20

7. The display apparatus according to claim 6, wherein n is two, the XY calculating circuit comprises two capacitors connected in series between the X signal line and the Y signal line, wherein the voltage of the connection node of two capacitors

09876119-060001

is input to the signal comparator as an output value, wherein the voltage VYMAX applied to Y signal line is a high voltage enough to allow the output of the XY arithmetic circuit to be higher than the reference voltage of the signal comparator regardless of the voltage applied to X signal line, wherein the voltage VYMIN applied to Y signal line is a high voltage enough to allow the output of the XY arithmetic circuit to be lower than the reference voltage of the signal comparator regardless of the voltage applied to X signal line, wherein VYMAX is applied to Y signal lines of the first to N-th rows, and VYMIN is applied to Y signal lines other than the first to Nth row, for the first selection period, wherein the voltage $VY1 < VY2 < \dots < VYN$ are applied to Y signal lines of the 1st to N-th rows, VYMAX is applied to Y signal lines of the (N+1)-th to 2N-th rows, and VYMIN is applied to Y signal lines other than the first to 2Nth rows, for the second selection period. Hereafter, for the i-th selection period, wherein the voltage $VY1 < VY2 < \dots < VYN$ are applied to Y signal lines of the $((i-2) \times N + 1)$ -th to $((i-1) \times N)$ -th rows, VYMAX is applied to Y signal lines of the $((i-1) \times N + 1)$ -th to $(i \times N)$ -th rows, and VYMIN is applied to Y signal lines other than the $((i-2) \times N + 1)$ -th to $(i \times N)$ -th rows.

8. The display method according to claim 1, wherein n is two, the XY calculating circuit comprises a capacitor of which one

terminal is connected to the Y signal line and the other terminal to a drain electrode, and a transistor of which a source electrode is connected to the X signal line;

wherein the voltage of the drain electrode of the transistor is input to the signal comparator as an output value, voltage VYMAX applied to Y signal line is a high voltage enough to allow the output of the XY arithmetic circuit to be higher than the reference voltage of the signal comparator regardless of the voltage applied to X signal line, voltage VYMIN applied to Y signal line is a high voltage enough to allow the output of the XY arithmetic circuit to be lower than the reference voltage of the signal comparator regardless of the voltage applied to X signal line, voltage VYMAX is applied to Y signal lines of the 1st to N-th rows, and VYMIN is applied to Y signal lines other than the first to N-th row, for the first selection period, the voltage $VY1 < VY2 < \dots < VYN$ are applied to Y signal lines of the first to N-th rows, VYMAX is applied to Y signal lines of the (N+1)-th to 2N-th rows, and VYMIN is applied to Y signal lines other than the first to 2N-th rows, for the second selection period. Hereafter, for the i-th selection period, the voltage $VY1 < VY2 < \dots < VYN$ are applied to Y signal lines of the $((i-2) \times N + 1)$ -th to $((i-1) \times N)$ -th rows, VYMAX is applied to Y signal line of the $((i-1) \times N + 1)$ -th to $(i \times N)$ -th rows, and VYMIN is applied to Y signal lines other than the $((i-2) \times N + 1)$ -th to $(i \times N)$ -th

T09090"6T9ZB60

9. The display apparatus according to claim 6, wherein n is two, the XY calculating circuit may comprise a capacitor of which one terminal is connected to the Y signal line and the other terminal to a drain electrode, and a transistor of which a source electrode is connected to the X signal line like the above-mentioned circuit, wherein the voltage of the drain electrode of the transistor is input to the signal comparator as an output value. The voltage V_{MAX} applied to Y signal line is a high voltage enough to allow the output of the XY arithmetic circuit to be higher than the reference voltage of the signal comparator regardless of the voltage applied to X signal line, voltage V_{MIN} applied to Y signal line is a high voltage enough to allow the output of the XY arithmetic circuit to be lower than the reference voltage of the signal comparator regardless of the voltage applied to X signal line, wherein V_{MAX} is applied to Y signal lines of the first to N-th rows, and V_{MIN} is applied to Y signal lines other than the first to N-th rows, for the first selection period. Next, the voltage $VY1 < VY2 < \dots < VYN$ are applied to Y signal lines of the first to N-th rows, and V_{MIN} is applied to Y signal lines other than the first to N-th rows, for the second selection period. Hereafter, for the $(2 \times i - 1)$ -th selection period ($i = 1, 2, 3, \dots$), V_{MAX} is applied to Y signal lines

of the $((i-1) \times N + 1)$ -th to $(i \times N)$ -th rows, and V_{YMIN} is applied to Y signal lines other than the $((i-1) \times N + 1)$ -th to $(i \times N)$ -th rows, wherein for the $(2 \times i)$ -th selection period, the voltage $V_{Y1} < V_{Y2} < \dots < V_{YN}$ are applied to Y signal lines of the $((i-1) \times N + 1)$ -th to $(i \times N)$ -th rows, and V_{YMIN} is applied to Y signal lines other than the $((i-1) \times N + 1)$ to $(i \times N)$ -th rows.

10. The display apparatus according to claim 6, wherein in each of N' columns in $i=1, 2, \dots, 3$ in such a display apparatus, wherein the liquid crystal drive voltage lines of the $((2 \times i - 2) \times N + 1)$ -th to $((2 \times i - 1) \times N)$ -th rows are connected to one another, the liquid crystal drive voltage lines of the $((2 \times i - 1) \times N + 1)$ -th to $(2 \times i \times N)$ -th rows is connected to one another, and the liquid crystal drive voltage lines of the $((2 \times i - 2) \times N + 1)$ -th to $((2 \times i - 1) \times N)$ -th rows and the liquid crystal drive voltage lines of the $((2 \times i - 1) \times N + 1)$ -th to $(2 \times i \times N)$ -th rows are not connected to one another.

11. The display apparatus according to claim 6, wherein n is two, and the XY calculating circuit comprises a capacitor of which one terminal is connected to the Y signal line and the other terminal to a drain electrode, and a transistor of which a source electrode is connected to the X signal line. In this case, the voltage of the drain electrode of the transistor is

input to the signal comparator as an output value, V_{MAX} and V_{MID} applied to Y signal line are set to a high voltage enough to allow the value of $V_X + V_{MAX} + V_{MID}$ to be higher than the reference voltage of the signal comparator regardless of the value of the voltage V_X applied to X signal line, V_{MIN} applied to Y signal line is set to a high voltage enough to allow the output of the XY arithmetic circuit to be lower than the reference voltage of the signal comparator regardless of the voltage applied to X signal line, wherein for the first selection period, V_{MID} is applied to Y signal lines of the first to N-th rows, V_{MIN} is applied to Y signal lines other than the first to N-th rows, wherein for the second selection period, V_{MAX} is applied to Y signal lines of the first to N-th rows. V_{MID} is applied to Y signal lines other than the (N+1)-th to 2N-th rows, V_{MIN} is applied to Y signal lines other than the first to 2N-th rows, wherein for the third selection period, the voltage $V_{Y1} < V_{Y2} < \dots < V_{YN}$ are applied to Y signal lines of the first to N-th rows, V_{MAX} is applied to Y signal lines of the (N+1)-th to 2N-th rows. V_{MID} is applied to Y signal lines of the (2N+1)-th to 3N-th rows, and V_{MIN} is applied to Y signal lines other than the first to 3N-th rows, and wherein for the i-th selection period, the voltage $V_{Y1} < V_{Y2} < \dots < V_{YN}$ are applied to Y signal lines of the ((i-1) × N + 1)-th to ((i-2) × N)-th rows, V_{MAX} is applied to Y signal lines of the ((i-2) × N + 1)-th to ((i-1) × N)-th rows, V_{MID} is

09876543210

applied to Y signal lines of the $((i-1) \times N+1)$ -th to $(i \times N)$ -th rows, and VYMIN is applied to Y signal lines other than the $((i-3) \times N+1)$ -th to $(i \times N)$ -th rows.

- 5 12. A display apparatus comprises:

red color pixel electrodes, green color pixel electrodes,
and blue color pixel electrodes arranged like a matrix;

display elements which operate according to the voltage of the pixel electrode;

10 an X driver for supplying an X signal to an X signal line
arranged in the column direction;

an Y driver for supplying a Y signal to a Y signal line
arranged in the row direction;

15 a liquid crystal drive voltage supplying circuit for
supplying a liquid crystal drive voltage to liquid crystal drive
voltage lines for red color, green color, and blue color arranged
in a column direction;

an XY calculating circuit provided at the intersection
parts of the X signal line and the Y signal line and connected
20 to the X signal line and the Y signal line for calculating and
outputting the X and Y signals;

a signal comparator for comparing an output of the XY calculating circuit with a reference voltage and outputting a first voltage when the the output of the XY calculating circuit

a switch for controlling the connection of the red color pixel electrode and the red color liquid crystal drive voltage line, based on the output of the signal comparator;

a switch for controlling the connection of the green color pixel electrode and the green color liquid crystal drive voltage line, based on the output of the signal comparator;

a signal control circuit for controlling the X driver, the Y driver, and the liquid crystal drive voltage supplying circuit, according to the n-gradation approximation picture signal.

13. The display apparatus according to claim 6, wherein said each pixel comprises:

a plurality of row lines arranged in a row direction, from which a VY signal is supplied;

5 a plurality of column lines arranged in a row direction, from which a VX signal is supplied;

pixel electrodes provided at intersection parts of row lines and column lines;

10 switching elements provided at the intersection parts of row lines and column lines, for controlling the connection of a data signal supply line and the pixel electrode, according to the calculating value of corresponding signal VX and signal VY.

15 14. The display apparatus according to claim 6, wherein said each pixel comprises;

a plurality of row lines arranged in a row direction, for supplying a signal VY;

20 a plurality of column lines arranged in a column direction, for supplying a signal VX;

a red color pixel electrode, a green color pixel electrode, and a blue color pixel electrode, each provided at intersection parts of a row line and a column line;

switching elements tp for controlling the connection of

0587619-060001

a red color data signal supply line and a red color pixel electrode,
 the connection of a green color data signal supply line and a
 green color pixel electrode, and the connection of a blue color
 data signal supply line and a blue color pixel electrode to be
 5 in the same state, according to the calculation value of the
 corresponding VX signal and VY signal.

15. A display system comprises:

the display apparatus according to claim 6;

10 a picture generating unit for instructing the display
 apparatus so as to display a picture; and

a display control for inputting the picture signal to the
 display apparatus according to the instruction;

15 wherein said display apparatus has a means for allocating
 the gradation of n values to each pixel of the pixel block formed
 from $N \times N'$ pixels.

16. A display system comprises:

the display apparatus according to claim 6;

20 a picture generating unit for instructing the display
 apparatus so as to display a picture; and

a display control for inputting the picture signal to the
 display apparatus according to the instruction;

wherein said display control has a means for allocating

0967619-0601
 103090-6190601

the gradation of n values to each pixel of the pixel block composed of $N \times N'$ pixels.

17. A display system comprises:

- 5 the display apparatus according to claim 6;
a picture generating unit for instructing the display apparatus so as to display a picture; and
a display control for inputting the picture signal to the display apparatus according to the instruction;
10 wherein said picture generating unit has a means for allocating the gradation of n values to each pixel of the pixel block composed of $N \times N'$ pixels.

18. A display apparatus comprises:

- 15 an X driver for supplying an X signal to an N_X X signal lines arranged in the column direction;
an Y driver for supplying a Y signal to a N_Y Y signal lines arranged in the row direction;
a signal control circuit for controlling said X driver
20 and said Y driver;
pixel electrodes provided at intersection parts of a X signal line and a Y signal line, and arranged like a matrix:
display elements which operates according to the voltage of the pixel electrode;

5